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EXAMINER

WANG, ALBERT C

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

1. Original claims 1-23 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7, 9-12, 15, 17-20 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumar et al., U.S. Patent No. 7,096,377 (“Kumar”).

As per claim 1, Kumar teaches a method in a multi-processor data processing system for changing an operating frequency for a system core logic used to interface to memory in the data processing system, the method comprising:

determining whether the operating frequency should be changed from a default frequency to another frequency (col. 1, lines 46-57, “... choose common clock speed that will enable all the components to work together”; col. 5, line 65 – col. 6, line 17, “... calculate a parameter value ... that would enable the processors, logic 320 and/or memory 330 to work together”, where system core logic normally runs at default frequency – e.g. see Applicant’s admitted prior art p. 2, lines 2-14);

responsive to determining the operating frequency should be changed from the default frequency to the another frequency, placing slave processors in the multi-processor data processing system into a non-transactional mode (col. 3, lines 1-34, in response to querying that

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occurs before placing processor in non-transactional mode; col. 4, lines 35-47; col. 5, lines 4-21, some processors are inherently designated as slave processors); and

changing the operating frequency in the system core logic to the another frequency (col. 5, line 65 – col. 6, line 17, “... set ... logic 320 with the calculated parameters ...”).

As per claim 2, Kumar teaches placing the slave processors into a normal mode (col. 5, line 65 – col. 6, line 17, processors would be in normal mode in order to work together).

As per claim 3, completing initialization of the multi processor data processing system normally occurs when there is no error.

As per claim 4, Kumar teaches the non-transactional mode is a sleep mode (col. 3, lines 1-21).

As per claim 7, Kumar teaches the determining step, the placing step, and the changing step are performed by a master processor in the multi-processor data processing system (col. 3, lines 1-21; col. 7, lines 6-41).

As per claim 9, Kumar teaches a multi-processor data processing, system for changing an operating frequency for a system core logic used to interface to memory in the multi-processor data processing system, the multi-processor data processing system comprising:

determining means for determining whether the operating frequency should be changed from the default frequency to the another frequency (col. 1, lines 46-57, “... choose common clock speed that will enable all the components to work together”; col. 5, line 65 – col. 6, line 17, “... calculate a parameter value ... that would enable the processors, logic 320 and/or memory

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330 to work together”, where system core logic normally runs at default frequency – e.g. see Applicant’s admitted prior art p. 2, lines 2-14);

placing means, responsive to determining the operating frequency should be changed from a default frequency to another frequency, for placing slave processors in the multi-processor data processing system into a non-transactional mode (col. 3, lines 1-34, in response to querying that occurs before placing processor in non-transactional mode; col. 4, lines 35-47; col. 5, lines 4-21, some processors are inherently designated as slave processors); and

changing means for changing the operating frequency in the system core logic to the another frequency (col. 5, line 65 – col. 6, line 17, “... set ... logic 320 with the calculated parameters ...”).

As per claims 10-12 and 15, since Kumar teaches the method of claims 1-4 & 7 and the system of claim 9, Kumar teaches the claimed system.

As per claims 17-20, since Kumar teaches the method of claims 1-4 & 7 and the system of claims 9-12 & 15, Kumar teaches the claimed program.

As per claim 23, Kumar teaches a data processing system comprising:
a bus system (figs. 1-3, busses connected to logic 120, 220, and 320);
a memory connected to the bus system, wherein the memory includes a set of instructions (figs. 1-3, memories 130, 230, and 330; col. 6, lines 41-57; boot or BIOS ROM is inherent – e.g. see Lee, U.S. Patent No. 5,867,702, fig. 1 and col. 2, line 57 – col. 3, line 10, boot code 176 in NVRAM 175); and

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a processing unit connected to the bus system, wherein the processing unit executes a set of instructions to determine whether the operating frequency should be changed from the default frequency to the another frequency (col. 1, lines 46-57, "... choose common clock speed that will enable all the components to work together"; col. 3, lines 1-21, processor executes instructions; col. 5, line 65 – col. 6, line 17, "... calculate a parameter value ... that would enable the processors, logic 320 and/or memory 330 to work together", where system core logic normally runs at default frequency – e.g. see Applicant's admitted prior art p. 2, lines 2-14);

place slave processors in the multi-processor data processing system into a non-transactional mode in response to determining the operating frequency should be changed from a default frequency to another frequency (col. 3, lines 1-34, in response to querying that occurs before placing processor in non-transactional mode; col. 4, lines 35-47; col. 5, lines 4-21, some processors are inherently designated as slave processors); and

change the operating frequency in the system core logic to the another frequency (col. 5, line 65 – col. 6, line 17, "... set ... logic 320 with the calculated parameters ...").

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5, 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar as applied to claims 1, 9, and 17 above, and further in view of Lee, U.S. Patent No. 5,867,658.

As per claims 5, 13 and 21, Kumar teaches the non-transactional mode is one of various possible modes in which the slave processors do not generating any external bus transactions (col. 3, lines 1-21; col. 5, lines 6-21), but does not expressly teach the non-transactional mode as being a spin loop. Lee teaches that being in a spin loop is one known form of non-transactional mode (col. 2, lines 52-67). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Lee's executing spin loop as Kumar's non-transactional mode, as executing a spin loop is a known alternative for halting a processor.

6. Claims 6, 8, 14, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar as applied to claims 1, 9, and 17 above, and further in view of Kurowasa, U.S. Patent No. 6,643,792.

As per claims 6, 14 and 22, Kumar does not expressly teach the changing step comprises setting a register in the system core logic to a value for the another frequency. Kurowasa teaches such details for a changing step (fig. 1, setting register R of clock generator within host PCI-bridge 6; col. 9, lines 4-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art that Kurowasa's register setting is applicable to Kumar's method, as such register setting is a common method for changing the operating frequency of system core logic.

As per claims 8 and 16, symmetric multiprocessing (SMP), in which identical processors share system memory, is well-known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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**CHUN CAO
PRIMARY EXAMINER**